

# SpaceWire Product Information

General Information	
This Data was Current On	July 12, 2010
Company Name	Levent Ozturk
IP Name	SpaceWire
IP Part Number	
Current IP Revision Number	6.2
Date Current Revision was Released	May 10, 2006
Release Date of first Version	May 16, 2002
Production Use by Customers	
Number of successful Customer production projects	2
Can references be made available?	Yes
Deliverables	
VSIA Quality IP (QIP) checklist completed and available?	
IP Formats available for purchase	Bitstream, Netlist, Source Code
Source Code Format(s)	Verilog
High-Level Model Included?	No
High-level Model Format(s)	
Integration Testbench Provided	Yes
Integration Testbench Format(s)	Verilog
Code Coverage Report Provided?	Yes
Functional Coverage Report Provided?	
Constraints File Provided?	Yes
Commercial Evaluation Board Available?	Yes
FPGA used on board	Virtex 6, Stratix IV
Software Drivers Provided?	No
Driver OS Support	
Implementation	
FPGA Optimization Techniques	Yes
Code Optimized for Vendor?	Altera, Xilinx
Synthesis Software Tools Supported / version	XST
Static Timing Analysis Performed?	Yes
Standard IP Interface(s) Supported	No
Metadata Included?	
Verification	
Is a documented verification plan available?	Yes
Test Methodology	Random, Incremental, Directed, Corner cases, stress cases
Assertions	Yes
Coverage Metrics Collected	Code
Timing Verification Performed?	
Timing Verification Report Available?	Yes
Simulators supported	Modelsim, Cadence NC-Sim
Hardware Validation	
Validated on FPGA	Altera Xilinx
Hardware validation platform used	
Industry standard compliance testing passed	
Specific compliance test Test date	
Are test results available?	

